8T SRAM cell design for Wide Voltage Range in 28nm FDSOI

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Abstract

This work focuses on Low-Power, High-Speed 8T SRAM bitcell design optimization under stability and yield constraints in 28nm FDSOI technology. To this end an investigation of existing dynamic stability metrics and their limitations is presented. In the analysis it is demonstrated that using standard writeability metric can be misleading, either overestimating or underestimating the real stability. Read-after-write emerges as the most accurate metric, overcoming the limitations of standard writeability evaluation. The analysis is performed using ICLYS- a tool from INFINISCALE, which is capable of performing accurate statistical simulations on any given input netlist with a significant speedup over a standard Monte Carlo simulation. The accuracy and speed advantage of ICLYS are validated and demonstrated as a part of this presentation.
Application motivations

Wireless applications:
- Low standby power
- Low operating power
- High speed

Accurate yield estimation:
- Long; new approaches needed

Low-power + High-Speed:
- Stability problems @low voltage
- Dynamic margins required

❃ Accurate, realistic and fast SRAM stability estimation ever more important
ICLys tool to reduce simulation burden

- Enhanced Monte Carlo analyses using smart sampling strategies
- High Sigma adaptive kernel to explore extremes up to 6 sigma

Fast and accurate for variation-aware design

http://www.infiniscale.com/
Very good agreement between both simulations
28nm FDSOI technology

① Gate stack
  - High-k (COX)
  - Metal-Gate ($V_T$)
② Raised-SD (RSD)
③ Si-film (~$L_G/4$)
  - No channel doping
  - No pocket implant
④ BOX (25nm)
⑤ Back plane ($V_T$)
⑥ Back biasing
⑦ Isolation (STI)

SPW-NW 8T bitcell

➲ Low variability planar Multiple-VT technology
➲ Wide range, independent back bias adjustment

N. Planes, VLSI 2012, O. Thomas SOICONF 2012, R. Ranica, VLSI 2013
**Standard dynamic bitcell metrics**

### Readability (RA)

Stable if:
- $\Delta V_{BL} \geq \Delta V_{BLMIN}$
- $\Delta V_{BLMIN}$ typically 100mV
- (sensing scheme dependant)

### Writeability (WA)

Stable if at the end of $T_{CLK}$:
- $V_{NODE_{PU}} > target$
- target = arbitrary value for which write is assumed as complete (e.g. 80% $V_{DD}$ or 60% $V_{DD}$)
Please contact us for the whole paper.